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EXAMINER	
DO, CHAT C	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,274	DENIS LEHONGRE	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003 and 20 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/03/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Election/Restriction filed 02/20/2007.

2. Claims 1-58 are pending in this application. Claims 1-2, 7-8, 15-16, 17-23, 31, 37, and 54 are independent claims. In response, claims 54-58 are added. This Office Action is made non-final.

Drawings

3. Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 1, 7, and 57 are objected to because of the following informalities:

Re claim 1, the applicant is advised to separate words "devicecomprising" as "device comprising" for clarification.

Re claim 7, it is missing a period at the end of the claim.

Re claim 57, it has same limitations cited in claim 55.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-58 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-58 cite a device for processing digital data in accordance with a mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application or a concrete, useful, and tangible result. However, claims 1-58 merely disclose steps/components for converting digital data to be processed without further disclosing a practical/physical application or a useful and tangible result since the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein. Therefore, claims 1-58 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-58 are rejected under 35 U.S.C. 102(b) as being anticipated by Imbert de Tremiolles et al. (U.S. 2001/0013048).

Re claim 1, Imbert de Tremiolles et al. disclose in Figures 2-6 a device for processing digital data belonging to a set of 2.sup.n codes in which a relation of order is established and in which each of data has a rank R comprised between 0 and 2.sup.n-1, device (e.g. abstract and Figure 4) comprising: a conversion circuit for each digital data to be processed, in order to generate a transform that is a binary number composed of 2.sup.n-1 binary elements T[x] with x=1 to 2.sup.n-1T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[2]T[1] wherein T(x)=0 when x is strictly higher than R and T(x)=1 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and circuits to receive a result of the conversions and to carry out a digital processing of result (e.g. other steps as seen in paragraphs [0015-0017]).

Re claim 2, it has similar limitations cited in claim 1 wherein x = 0 and start at T[0] (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]). Thus, claim 2 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 3, Imbert de Tremiolles et al. further disclose in Figures 2-6 characterized in that digital processing is a Boolean OR carried out in bit-serial way on bits of same index of the transformed data and followed by a conversion which is a reverse of transform, in order to read out a maximum value of a set of digital values (e.g. paragraph [0014]).

Re claim 4, Imbert de Tremiolles et al. further disclose in Figures 2-6 the read out of maximum value is followed by a comparison with another value (e.g. abstract and paragraph [0011]).

Re claim 5, Imbert de Tremiolles et al. further disclose in Figures 2-6 digital processing is a Boolean AND, carried out in a bit-serial way on bits of same index of the transformed data and followed by a conversion which is a reverse of transform, in order to read out a minimum value of a set of digital values (e.g. paragraphs [0011-0017]).

Re claim 6, it has similar limitations cited in claim 4. Thus, claim 6 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 7, it has similar limitations cited in claim 1 wherein x = 1 and start at T[1]; T(x) =1 and T(x) = 0 respectively (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]). Thus, claim 7 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 8, it has similar limitations cited in claim 1 wherein x = 0 and start at T[0]; T(x) 1 and T(x) = 0 respectively (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]). Thus, claim 8 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 9, it has similar limitations cited in claim 5. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 10, it has similar limitations cited in claim 6. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 11, it has similar limitations cited in claim 3. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 12, it has similar limitations cited in claim 4. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 13, Imbert de Tremiolles et al. further disclose in Figures 2-6 the original code of the digital data to process is of the signed type, not signed, Gray, Johnson or includes a mantissa and an exponent (e.g. Figures 2).

Re claim 14, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. by feedback loop for all the sub-group in Figure 4).

Re claim 15, it has similar limitations cited in claim 3. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 16, Imbert de Tremiolles et al. further disclose in Figures 2-6 a device for reading out a maximum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R comprised between 0 and 2.sup.n-1 (e.g. abstract and Figure 4), device comprising: a circuit to represent each one of digital data under a form of a code made up of 2.sup.n

binary elements T[x] with x=0 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[1]T[0] wherein T(x)=0 when x is strictly higher than R and T(x)=1 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and logic circuits to carry out a logical OR in a bit-serial way on bits of same index of digital data, in order to read out the maximum of set of digital data (e.g. paragraphs [0011-0017]).

Re claim 17, Imbert de Tremiolles et al. further disclose in Figures 2-6 a device for reading out a minimum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R comprised between 0 and 2.sup.n-1, device (e.g. abstract and Figure 4) comprising: a circuit to represent each one of digital data under a form of a code made up of 2.sup.n-1 binary elements T[x] with x=1 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[2]T[1] wherein T(x)=0 when x is strictly higher than R and T(x)=1 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]) ; and logic circuits to carry out a logical AND in a bit-serial way on bits of same index of digital data, in order to read out the minimum of set of digital data (e.g. paragraphs [0011-0017]).

Re claim 18, Imbert de Tremiolles et al. further disclose in Figures 2-6 a device for reading out a minimum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R comprised between 0 and 2.sup.n-1 (e.g. abstract and Figure 4), device comprising: a circuit to represent each one of digital data under a form of a code made up of 2.sup.n

binary elements T[x] with x=0 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[1]T[0] wherein T(x)=0 when x is strictly higher than R and T(x)=1 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]) ; and logic circuits to carry out a logical AND in a bit-serial way on bits of same index of digital data, in order to read out the minimum of set of digital data (e.g. paragraphs [0011-0017]).

Re claim 19, Imbert de Tremiolles et al. further disclose in Figures 2-6 a device for reading out a maximum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R comprised between 0 and 2.sup.n-1 (e.g. abstract and Figure 4), device comprising: a circuit to represent each one of digital data under a form of a code made up of 2.sup.n-1 binary elements T[x] with x=1 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[2]T[1] wherein T(x)=1 when x is strictly higher than R and T(x)=0 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and logic circuits to carry out a logical AND in a bit-serial way on bits of same index of digital data, in order to read out the maximum of set of digital data (e.g. paragraphs [0011-0017]).

Re claim 20, Imbert de Tremiolles et al. further disclose in Figures 2-6 a device for reading out a maximum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R comprised between 0 and 2.sup.n-1 (e.g. abstract and Figure 4), device comprising: a circuit to represent each one of digital data under a form of a code made up of 2.sup.n

binary elements T[x] with x=0 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[1]T[0] wherein T(x)=1 when x is strictly higher than R and T(x)=0 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and logic circuits to carry out a logical AND in a bit-serial way on bits of same index of digital data, in order to read out the maximum of set of digital data (e.g. paragraphs [0011-0017]).

Re claim 21, Imbert de Tremiolles et al. further disclose in Figures 2-6 a device for reading out a minimum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R comprised between 0 and 2.sup.n-1 (e.g. abstract and Figure 4), device comprising: a circuit to represent each one of digital data under a form of a code made up of 2.sup.n-1 binary elements T[x] with x=1 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[2]T[1] wherein T(x)=1 when x is strictly higher than R and T(x)=0 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and logic circuits to carry out a logical OR in a bit-serial way on bits of same index of digital data, in order to read out the minimum of set of digital data (e.g. paragraphs [0011-0017]).

Re claim 22, Imbert de Tremiolles et al. further disclose in Figures 2-6 a device for reading out a minimum among a set of digital data belonging to a set of 2.sup.n codes in which a relation of order is established and for which each of data has a rank R comprised between 0 and 2.sup.n-1 (e.g. abstract and Figure 4), device comprising: a circuit to represent each one of digital data under a form of a code made up of 2.sup.n

binary elements T[x] with x=0 to 2.sup.n-1:T[2.sup.n-1]T[2.sup.n-2] . . . T[x] . . . T[1]T[0] wherein T(x)=1 when x is strictly higher than R and T(x)=0 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and logic circuits to carry out a logical OR in a bit-serial way on bits of same index of digital data, in order to read out the minimum of set of digital data (e.g. paragraphs [0011-0017]).

Re claim 23, Imbert de Tremiolles et al. further disclose in Figures 2-6 an apparatus (e.g. abstract and Figure 4), comprising: a conversion circuit to receive digital data belonging to a set of codes in which a relation of order is established and in which each of the digital data has a rank (e.g. Figure 4 and paragraphs [0012-0014]), the conversion circuit being capable to transform the received digital data into a binary number having binary elements whose values are based at least in part on a value of the rank; and a processing circuit coupled to the conversion circuit to receive the digital data that has been transformed to the binary number and to generate a result therefrom (e.g. paragraphs [0011-0017]).

Re claim 24, Imbert de Tremiolles et al. further disclose in Figures 2-6 the conversion circuit includes a plurality of conversion units, each being capable to transform their respective digital data from the set into a binary number (e.g. Figures 2-4).

Re claim 25, Imbert de Tremiolles et al. further disclose in Figures 2-6 the processing circuit (e.g. Figure 4 and abstract) includes: a first unit coupled to the conversion circuit to apply a logical operation on binary numbers received from the

conversion circuit to generate at least one output therefrom (e.g. Figures 2); and a second unit coupled to the first unit to perform a reverse transform on the at least one output from the first unit to generate the result (e.g. paragraphs [0007-0027]).

Re claim 26, Imbert de Tremiolles et al. further disclose in Figures 2-6 the logical operation comprises a logical OR operation carried out in a bit-serial manner on bits of the binary numbers of same index (e.g. paragraph [0014]).

Re claim 27, Imbert de Tremiolles et al. further disclose in Figures 2-6 the logical operation comprises a logical AND operation carried out in a bit-serial manner on bits of the binary numbers of same index (e.g. paragraph [0014]).

Re claim 28, Imbert de Tremiolles et al. further disclose in Figures 2-6 the result includes a minimum value of the set of digital data (e.g. abstract).

Re claim 29, Imbert de Tremiolles et al. further disclose in Figures 2-6 the result includes a maximum value of the set of digital data (e.g. abstract).

Re claim 30, Imbert de Tremiolles et al. further disclose in Figures 2-6 at least another circuit coupled to the processing circuit to compare the result with another value (e.g. Figures 2).

Re claim 31, Imbert de Tremiolles et al. further disclose in Figures 2-6 a method (e.g. abstract and Figure 4), comprising: receiving digital data belonging to a set of codes in which a relation of order is established and in which each of the digital data has a rank (e.g. step A in Figure 4); transforming each of the received digital data into a binary number having binary elements whose values are based at least in part on a value of the rank (e.g. steps B - step D in Figure 4); and processing the digital data that has been

transformed into the binary numbers to generate a result therefrom (e.g. output of Figure 4).

Re claim 32, Imbert de Tremiolles et al. further disclose in Figures 2-6 processing the digital data that has been transformed into the binary numbers (e.g. abstract and Figure 4) includes: applying a logical operation on the binary numbers to generate at least one output therefrom (e.g. paragraphs [0011-0017]); and performing a reverse transform on the at least one output to generate the result (e.g. paragraphs [0007-0027]).

Re claim 33, Imbert de Tremiolles et al. further disclose in Figures 2-6 applying the logical operation includes applying a logical OR operation in a bit-serial manner on bits of the binary numbers of same index (e.g. paragraph [0014]).

Re claim 34, Imbert de Tremiolles et al. further disclose in Figures 2-6 applying the logical operation includes applying a logical AND operation in a bit-serial manner on bits of the binary numbers of same index (e.g. paragraph [0014]).

Re claim 35, Imbert de Tremiolles et al. further disclose in Figures 2-6 generating the result includes at least one of generating a maximum and a minimum value of the set of digital data (e.g. paragraphs [0011-0012]).

Re claim 36, Imbert de Tremiolles et al. further disclose in Figures 2-6 comparing the generated result with another value (e.g. Figures 2).

Re claim 37, Imbert de Tremiolles et al. further disclose in Figures 2-6 an apparatus (e.g. Figure 4 and abstract), comprising: a means for receiving digital data belonging to a set of codes in which a relation of order is established and in which each of the digital data has a rank (e.g. Figure 4 and paragraphs [0011-0013]); a means for

transforming each of the received digital data into a binary number having binary elements whose values are based at least in part on a value of the rank (e.g. encoder in paragraph [0014]); and a means for processing the digital data that has been transformed into the binary numbers to generate a result therefrom (e.g. other steps in Figure 4).

Re claim 38, Imbert de Tremiolles et al. further disclose in Figures 2-6 the means for processing the digital data that has been transformed into the binary numbers includes: a means for applying a logical operation on the binary numbers to generate at least one output therefrom; and a means for performing a reverse transform on the at least one output to generate the result (e.g. output of Figure 4).

Re claim 39, Imbert de Tremiolles et al. further disclose in Figures 2-6 the means for applying the logical operation includes at least one of a means for applying a logical OR operation and a logical AND operation in a bit-serial manner on bits of the binary numbers of same index (e.g. paragraph [0014]).

Re claim 40, Imbert de Tremiolles et al. further disclose in Figures 2-6 the means for processing the digital data to generate the result includes at least one of a means for generating a maximum and a minimum value of the set of digital data (e.g. abstract and Figure 4).

Re claim 41, Imbert de Tremiolles et al. further disclose in Figures 2-6 a means for comparing the generated result with another value (e.g. Figures 2).

Re claim 42, Imbert de Tremiolles et al. further disclose in Figures 2-6 digital processing is a Boolean OR, carried out in bit-serial way on the bits of same index of the

transformed data and followed by a conversion which is the reverse of transform, in order to read out the maximum value of a set of digital values (e.g. paragraphs [0007-0027]).

Re claim 43, Imbert de Tremiolles et al. further disclose in Figures 2-6 digital processing is a Boolean AND, carried out in a bit-serial way on the bits of same index of the transformed data and followed by a conversion which is the reverse of transform, in order to read out the minimum value of a set of digital values (e.g. paragraphs [0007-0027]).

Re claim 44, Imbert de Tremiolles et al. further disclose in Figures 2-6 a digital processing is a Boolean AND, carried out in a bit-serial way on the bits of same index of the transformed data and followed by a conversion which is the reverse of transform, in order to read out the maximum value of a set of digital values (e.g. paragraphs [0007-0027]).

Re claim 45, Imbert de Tremiolles et al. further disclose in Figures 2-6 digital processing is a Boolean OR, carried out in a bit-serial way on the bits of same index of the transformed data and followed by a conversion which is the reverse of transform, in order to read out the minimum value of a set of digital values (e.g. paragraphs [0007-0027]).

Re claim 46, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 47, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 48, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 49, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 50, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 51, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 52, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 53, Imbert de Tremiolles et al. further disclose in Figures 2-6 transform is applied only to a sub-group of binary elements of each data, in order to process in sequence various parts of each data (e.g. Figures 2-4).

Re claim 54, Imbert de Tremiolles et al. further disclose in Figures 2-6 a device for processing digital data belonging to a se of 2n codes in which a relation of order is established and in which each of data has a rank R comprised between 0 and 2n-1 (e.g. abstract and Figure 4), the device comprising: a conversion circuit for each digital data to be processed, in order to generate a transform that is a binary number composed of 2n-1 binary elements T[x] with x=a to 2n-1 with a and b being equal to 0 or 1, wherein T(x) = 0 when x is strictly higher than R and T(x) = 1 when x is lower or equal to R (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]); and circuits to receive a result of the conversions and to carry out a digital processing of the circuit (e.g. paragraphs [0011-0017]).

Re claim 55, Imbert de Tremiolles et al. further disclose in Figures 2-6 (a,b) = (1,1) (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]).

Re claim 56, Imbert de Tremiolles et al. further disclose in Figures 2-6 (a,b) = (0,0) (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]).

Re claim 57, Imbert de Tremiolles et al. further disclose in Figures 2-6 (a,b) = (1,1) (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]).

Re claim 58, Imbert de Tremiolles et al. further disclose in Figures 2-6 (a,b) = (1,0) (e.g. encoding the sub-values in step C in Figure 4 and paragraph [0014]).

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection

is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 1-58 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 9 and 17-18 of copending Application No. 11/039,644. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

> Claims 9 and 17-18 of Application No. 11/039,644 contains every element of claims 1-58 of the instant application and thus anticipated the claims of the instant application. Claims of the instant application therefore are not patently distinct from the earlier patent claims and as such are unpatentable over obvious-type double patenting. A later patent/application claim is not patentably distinct from an earlier claim if the later claim is anticipated by the earlier claim.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARB LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

"Claim 12 and Claim 13 are generic to the species of invention covered by claim 3 of the patent. Thus, the generic invention is **"anticipated"** by the species of the patented invention. Cf., Titanium Metals Corp. v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (holding that an earlier species disclosure in the prior art defeats any generic claim) 4 . This court's predecessor has held that, without a terminal disclaimer, the species claims preclude issuance of the generic application. In re Van Ornum, 686 F.2d 937, 944, 214 USPQ 761, 767 (CCPA 1982); Schneller, 397 F.2d at 354. Accordingly, absent a terminal disclaimer, claims 12 and 13 were properly rejected under the doctrine of obviousness type double patenting." (In re Goodman (CA FC) 29 USPQ2d 2010 (12/3/1993).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,295,226

b. U.S. Patent No. 6,748,405

c. U.S. Patent No. 2005/0182878

d. U.S. Patent No. 4,012,627

e. U.S. Patent No. 6,647,449

f. U.S. Patent No. 6,779,014

g. U.S. Patent No. 6,760,742

h. U.S. Patent No. 6,985,985

i. U.S. Patent No. 7,043,514

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

November 13, 2007